A Security Alarm Design

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***Abstract*—This article will describe the design considerations and operating behavior of the security alarm system being developed by the second year class.**

***Index Terms*—alarm, keypad, security**

I. Introduction

EVERY 2nd year, student is expected to design and construct a security alarm system as part of the Digital Electronics course. The circuit is based on a description found in the text *Digital Fundamentals* by Floyd.

Students are expected to work independently and are provided assistance in interpreting datasheets but only general guidelines in implementing system requirements. Each student's approach in solving certain technical problems may therefore be unique.

The principle objective is not to reproduce a specific design, but rather to help students develop their own logical thinking ability.

II. Basic Operation

The alarm system has two operating modes: normal operation and programming mode.

A. Operating Mode

The operating mode can be divided into two states: armed and disarmed. To change from one state to the other requires entering a 4-digit code. If the incorrect code is entered, the system resets itself and will not change states.

The alarm system can easily be modified to include a single key arming feature so that the system can be armed without giving all personnel the arming/disarming code.

In the disarmed state, all security sensor data is ignored. In the armed stated, sensor data can be used to trigger an alarm. This may be either an audible or silent alarm.

1) 1st Timing Period

When a key is pressed, the memory address is incremented, the decoded key value is stored in Register A, and the value stored in memory shifted to Register B.

2) 2nd Timing Period

The values in Registers A and B are presented to a 4-bit comparator. This comparison is not made during the 1st timing period since the A and B inputs arrive at slightly different times. If the two values are equal, the comparator output goes high. This is gated by the 2nd one-shot pulse and increments the memory address counter and the output 4-digit counter.

The comparator output is also inverted and gated with the 2nd one-shot. This provides a positive reset pulse when A ≠ B. This pulse resets the memory address and 4-digit counters.

3) 3rd Timing Period

During the operating mode, the alarm system will toggle between armed and disarmed when four consecutive correct numbers are entered.

The output of this counter is gated with the output of the 3rd one-shot to create another reset pulse. This pulse resets the memory address counter and the output 4-digit counter.

A JK flip-flop at the output of the 4-digit counter toggles between the armed and disarmed states.

B. Programming Mode

The alarm system can store a 16-digit code, but for the sake of this project, the code length has been limited to 4-digits.

A toggle switch is used to enter the programming mode. To store a specific digit, one merely has to press the desired key and then press the STORE button. Once the entire code has been entered, the toggle switch is placed in the normal operating mode and the system is automatically reset.

These switches are normally located in the alarm panel and not at the entry keypads. A separate keypad at the alarm panel is normally provided to facilitate programming.

III. Circuit Details

A. Keypad Encoder

This design uses a 16 key keypad. The rows and columns from the keypad must be encoded into binary. This function is performed by a MM74C92 encoder.

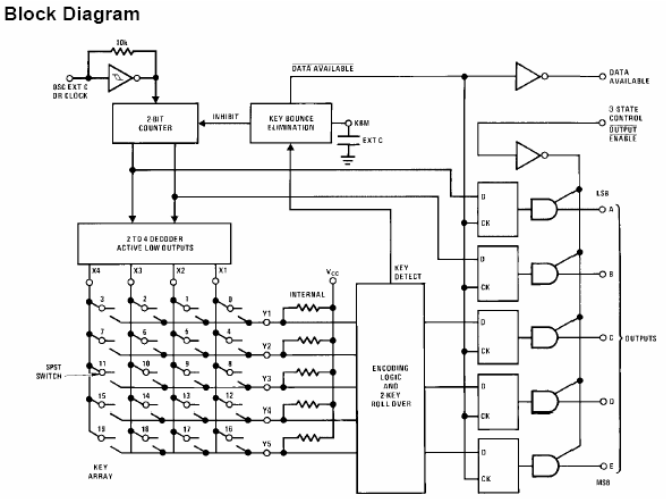

Fig. 1. MM74C92 Block Diagram

The MM74C92 encoder scans the keypad rows and columns, to determine which key is pressed. The result is fed to a latch and tri-state output. The tri-state output allows several keypads to be connected in parallel, thus allowing the alarm system to be controlled from several different locations. One of those locations would be at the alarm panel itself in order to facilitate programming. This feature however, was not implemented in this particular design.

The keypad scanning rate is determined by a capacitor to control a local oscillator on the encoder chip.

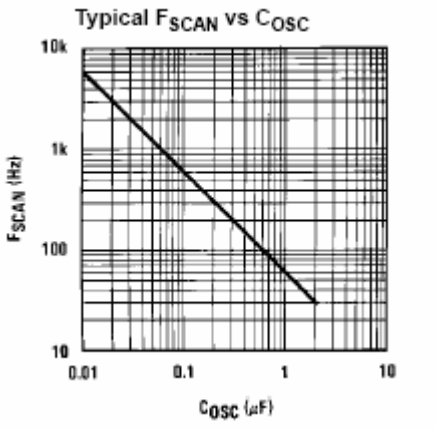

Fig. 2. Keypad scan rate capacitor

In this design, a value of 0.1μfd was selected to provide a scanning rate of approximately 1000 scans per second.

The keypad switches have a tendency to bounce, thus giving the impression that the key has been pressed several times in quick succession. To prevent this from happening, a debounce capacitor is used.

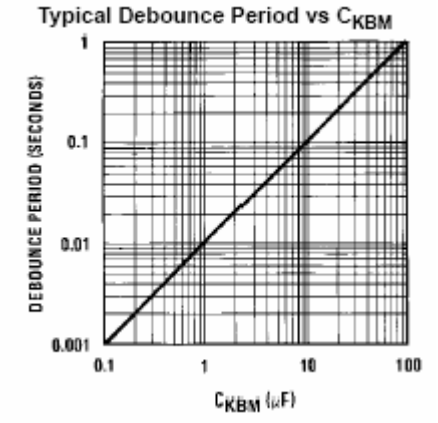

Fig. 3. Debounce capacitor

In this design, a value of 1μfd was selected to provide a debounce time of approximately 10 mSec.

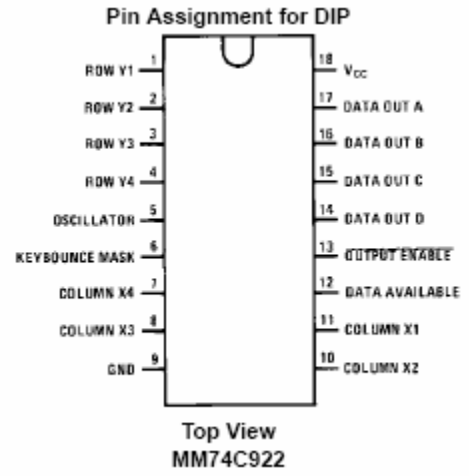

Fig. 4. MM74C92 Pin Assignment

B. Memory

A 74F189 64-bit RAM chip is used to store the entry code.

The address inputs are connected to a 74LS90 counter. The output of Register A is connected to the data inputs. The memory output is applied to a 74HCT540 inverter before going to Register B.

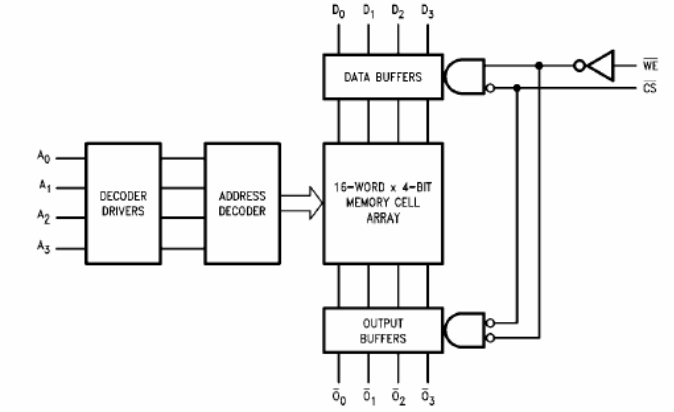

Fig. 5 74F189 RAM Block Diagram

1) Memory Addressing

In order to make certain that each entry is properly managed, the digits must be stored in sequence starting from some predetermined location. This is accomplished by means of a 74LS93 4-bit counter.

This counter is incremented during the 1st timing period when a key is pressed. This allows each digit to be stored sequentially.

The memory address counter is reset to zero under the following conditions:

1. The system has entered the Program Mode
2. The system has entered the Operating mode
3. An incorrect digit has been entered. (This condition is tested during the 2nd timing period in the Operating Mode.)
4. The complete code has correctly been entered. (This condition is tested during the 3rd timing period in the Operating Mode.)

2) Memory Programming

Inputs		Operation	Condition of Outputs
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

Fig. 6 74F189 Function Table

Since no other device will be placed in parallel with the memory outputs, the inhibit mode is not used in this circuit.

In order to store a value, the mode switch must be set to Programming. This resets the memory address counter, enables the store push button, and disables the other signals that would normally cause a reset.

The programming sequence is:

1. Toggle the switch to Programming Mode.
2. Press a Key.
3. Press Store
4. Press the next key
5. Press Sore (etc.)
6. When the last value has been stored, toggle the switch to the Operating Mode.

Switching back to the Operating mode will reset the memory address counter, disable the store push button, and re-enable the other reset signals.

C. Digit Comparison

A SM74LS85 4-bit magnitude comparator is used to check if the values in Register A and B are equal. This is achieved by setting all of the cascading input high.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

Fig. 5 74LS85 Truth Table.

Because the values from Registers A and B arrive at different times, it is necessary to gate the output at a time when both inputs are valid. This occurs during the 2nd timing period.

If A = B, a positive pulse is created to increment the memory address and 4-digit counters.

The comparator output is also passed through an inverter and gated to create a positive pulse if A ≠ B. This is used to reset the memory address and 4-digit counters.

IV. Acknowledgment

The author gratefully acknowledge the contributions of T. L. Floyd for suggesting this project.

V. References

Data Sheets:

[1] SN74LS74A, *Dual D-Type Positive Edge-Triggered Flip-Flop*, http://www.onsemi.com

[2] SN74LS85, *4-Bit Magnitude Comparator*, http://www.onsemi.com

[3] SN74LS90, *Decade Counter*, http://www.onsemi.com

[4] DM74121, *One-Shot with Clear and Complementary Outputs*, http://www.fairchild.com

[5] 74F189, *64-Bit RAM*, http://www.fairchild.com

[6] SN74LS195A, *Universal 4-Bit Binary Counter*, http://www.onsemi.com

[7] MM74HCT540, *Inverting Octal 3-State Buffer*, http://www.fairchild.com

[8] MM74C922, *16-Key Encoder*, http://www.fairchild.com

Books:

[9] T. L. Floyd, Digital Fundamentals 8th edition, 2003, Prentice-Hall.

VI. Biography

Roland Jugandi specializes in the telecommunication stream courses. He spent 12 years in research and development before going into academia. He has worked at the University of Winnipeg, SED Systems in Saskatoon, and Bell-Northern Research in Ottawa.

He has worked on nuclear instrumentation, sounding rockets, a UHF radiometer, mastitis detector, power converters, DMS-100 line cards, fiber services terminal and an assortment of other devices.